REMARKS

This Amendment, submitted in response to the Office Action dated February 26, 2004, is believed to be fully responsive to each point of rejection raised therein. Accordingly, favorable reconsideration on the merits is respectfully requested.

Claims 1-18 remain pending in the application. Claims 1-5, 7-12 and 14-15 have been rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Yamada and JP '954 (both previously of record) and further in view of Priem et al. (U.S.P. 4,908,780, hereafter "Priem"). Claims 6 and 13 have been rejected under 35 U.S.C. § 103 as being unpatentable over Yamada in view of JP '954 and Priem and further in view of Nakayoshi et al. (U.S.P. 6,310,667, hereafter "Nakayoshi"). Claim 16 has been rejected under 35 U.S.C. § 103 as being unpatentable over Yamada in view of JP '954 and Priem and further in view of Blakenbecler et al. (U.S.P. 6,104, 445, hereafter "Blakenbecler"). Claim 17 has been rejected under 35 U.S.C. § 103 as being unpatentable over Yamada in view of JP '954 and Priem and further in view of Tomiyasu. Claim 18 has been rejected under 35 U.S.C. § 103 as being unpatentable over Yamada in view of JP '954, Priem, Tomiyasu and Cok. Applicant submits the following comments in traversal of the prior art rejections.

Applicant's invention relates to a monochromatic display apparatus. Detailed descriptions of the background and exemplary embodiment of the invention are set forth in the January 26, 2004 Amendment at pages 6-7. Similarly, Yamada and JP '954 are described in the January 26 Amendment at page 7. Applicant refers the Examiner to these descriptions.

Further to these descriptions, Applicant would emphasize that to the extent that sub-pixels could be formed from a main pixel image, conventional devices required multiple drivers

or video cards in order to provide the sub-pixel output. This would also be a fundamental problem of the JP '954 reference. For example, in providing outputs to cels 41a, 41b and 41c, each cel individually has a time modulator element 12 and an on/off controller 13. Paragraph 26. None of the cited references include this object of the invention.

By contrast, the present invention permits a single card or set of image data to provide the multiple pixel output. In an exemplary embodiment, a base sub-pixel value is used as a reference for another sub-pixel value, and a differential output is provided as a 1 or 0 value to provide the different sub-pixel values. The reproduced image data corresponding to a certain step of gradation for one of the sub-pixels is thus used for displaying a transferred image, the transferred image being expressed as multiple sub-pixel values which can be different from each other.

Turning to the newly cited art, Priem relates to an anti-aliasing device to control pixel shading. In relevant part, Priem acknowledges that an output of a diagonal line as illustrated by Fig. 4a will have a jagged edge appearance in comparison to an anti-alias output as shown in Fig. 4b. Priem relates to an anti-alias output which divides a pixel into sub-pixels and controls the output of the sub-pixels to have an output color value that mitigates against aliasing visual effects. One pixel becomes divided into 16 sub-pixels as separate bit information. Col. 5, lines 36-37. To process one row of the sub-pixel information, discrete signals Sn, Sn+1, Sn+2 and Sn+3 are provided as inputs to multiplexers 84-87. Col. 6, lines 15-30. Based on a state of the sub pixel (See Fig. 5), a selection via signals Sn... Sn+3 determines a multiplexer output. Col. 6, lines 39-47. A logical combination of the multiplexer output with mask data AAMask in logic gates 80-83 and processing by filter 38 results in 8 output values AA0-AA7. The output values are provided to data latches 46...60 (Fig. 2) for determination of the saturation value for a pixel.

Moreover, the display of Priem handles data of binary form and cannot handle the number of steps of gradation as varied in sub-pixels as in the invention.

The Examiner contends that the combination of Yamada, JP '954 and Priem teaches or suggests each feature of claim 1. The rejection is not supported for at least four reasons.

First, as an initial matter, the Examiner continues to contend that the combination of Yamada and JP '954 would be motivated by a desire to provide a higher gradation. It has previously been submitted that the temporal requirements for error diffusion in the Yamada reference would not be compatible with the time modulation to provide the sub-pixel output as taught in JP '954 without a significant redesign of each reference. The Examiner has not responded to this argument. Therefore, Applicant would maintain that the combination is not supportable. For instance, to provide diffusion of error from a main pixel to adjacent pixels would require a first processing delay in Yamada. Meanwhile, JP '954 would teach a time-modulated output of the sub-pixels for the main image. Without a mutual redesign of each reference, the output would potentially result in spotty flicker in the error diffusive elements and the sub-pixels of the primary pixel, thereby detracting from the overall image appearance. There can be no motivation to combine the selective features cited by the Examiner.

Second, and relatedly, the error-diffusion approach in Yamada is also not conducive to the anti-aliasing of Priem. Priem relies on the appearance or lack of appearance of a data point in a sub-pixel in order to provide the appropriate masking and anti-aliasing filter output. However, with the error diffusion contemplated by the primary Yamada reference, the diffusion data may place a data point where none was intended in a sub-pixel in Priem, which would alter

the mask and anti-aliasing selection in a manner not contemplated by the Priem reference. At a most basic level, the error diffusion of Yamada is not compatible with either JP '954 or Priem, and the obviousness rejection is not supported for at least this reason.

Third, even assuming *arguendo* the references can be combined, their combination does not teach each aspect of independent claim 1. Claim 1 describes sub-pixels of different gradation of a transferred image, and also reproducing the transferred image data (having multiple gradations of sub-pixels) using the same number of steps of gradation of one of the sub-pixels. In essence, based on a gradation of one of the sub-pixel, the transferred image (having multiple sub-pixel values) can be reproduced. This feature is lacking in Yamada and Priem. In Yamada, the sub-pixel information is provided by modulation of separate timing modulators and separate on/off controllers. Therefore, the multiple image data are based on separate drivers and separate data, rather than image data having gradation of one of the sub-pixels. In Priem, the sub-pixel information also requires separate data Sn... Sn+3 and separate drivers, and not reproduction of the transferred image data based on gradation of one of the sub-pixels.

Fourth, the Examiner's reliance on JP '954 (paragraphs 53, 59) to teach the reproduction of the transferred image based on gradation of one of the sub-pixels is incorrect due to the presence of separate data drivers to replicate the multiple sub-pixel levels. The Examiner's reliance on cols. 5-6 of Priem is similarly deficient. Therefore, the combination of Yamada, JP '954 and Priem does not support the rejection.

Because independent claim 9 includes features discussed above for claim 1, claim 9 is patentable for the reasons set forth above. The remaining claims are patentable based on their dependency.

With further regard to claims 2 and 10, these claims describe differential data in relation to one sub-pixel to supply the other sub-pixel information. The Examiner cites Yamada to teach this feature. However, since Yamada concededly does not teach sub-pixels, it is not possible for Yamada to teach differential data to obtain sub-pixel information. The Examiner's reliance on JP '954, paragraphs 6-7 does not teach feature of claims 2 and 10. Paragraphs 6-7 only describe multiple gradation levels without reference to differential values.

With further regard to claim 3, this claim describes that one of the sub-pixels is represented as one bit. The Examiner's reliance on paragraphs 59, 60 and 63-64 of JP '954 to teach this feature is not supported. JP '954 teaches an 8bit representation for each subpixel. See Tables.

With further regard to claims 7 and 14, these claims describe a single video card for driving multiple displays. To the extent video cards are known, the prior art does not teach using the driving arrangement for multiple displays in combination with the remaining features of claims 1 and 9. Therefore, claims 7 and 14 are patentable for this additional reason.

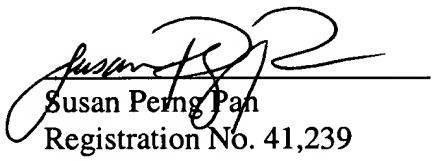
With further regard to claims 6, 13 and 16-18, the additional references of Nakayoshi, Tomiyasu, Blakenbecler and Cok do not make up for the deficiencies of the primary combination.

Applicant has added claims 19-22 to describe the invention more particularly.

In view of the above, Applicant submits that claims 1-22 are in condition for allowance. Therefore it is respectfully requested that the subject application be passed to issue at the earliest possible time. The Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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